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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/708,430	03/03/2004	Michael P. Belyansky	FIS920030245	2429

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EXAMINER	
HUYNH, ANDY	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/708,430	BELYANSKY ET AL.	
	Examiner	Art Unit	
	Andy Huynh	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22,24,25 and 31-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22, 24, 25 and 31-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *05/11/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after allowance or after an Office action under *Ex Parte Quayle*, 25 USPQ 74, 453 O.G. 213 (Comm'r Pat. 1935). Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, prosecution in this application has been reopened pursuant to 37 CFR 1.114. Applicant's submission filed on May 11, 2006 has been entered.

In the Amendment filed May 11, 2006, new claims **38-47** have been added. Claims **23 and 26-30** have been canceled. Accordingly, claims **1-22, 24, 25 and 31-47** are currently pending in this application.

Allowable Subject Matter

The indicated allowability of Claims **1-22, 24, 25 and 31-37** is withdrawn in view of the newly discovered reference(s). Rejections based on the newly cited reference(s) follow.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed 05/11/2006 and made of record. The references cited on the PTOL 1449 form have been considered.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims **1, 3-5, 9-18 and 31-37** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (USP 6,111,292 hereinafter referred to as "Gardner") in view of Murthy et al. (US 6,621,131 hereinafter referred to as "Murthy").

Regarding Claims **1, 3, 4 and 10-13**, Gardner discloses in Figs. 7-11 and the corresponding texts as set forth in column 6, line 40-column 9, line 29, a method of forming a semiconductor structure comprises steps of:

forming spacer voids/openings 46 between a gate 44 and a mandrel/dielectric layer 34;

creating recesses/LDD areas 48 in a substrate 30 below and in alignment with the spacer voids/the openings; and

removing the mandrel/dielectric layer;

wherein the recesses include a first recess and a second recess, the first recess and the second recess having a depth greater than a depth of the bottom of a channel area of the gate, and wherein the first recess has a depth substantially equal to the depth of the second recess.

Gardner fails to teach a method of forming a semiconductor structure comprises steps of filling a first portion of recesses with a stress imposing material; and filling a second portion of the recesses with a semiconductor material. Murthy teaches in Figs. 5-7 a method of forming a

semiconductor transistor having a stressed channel, comprises the steps of forming recesses 36A, 36B in a substrate 10; filling a first portion of recesses with a stress imposing material 22A, 22B; and filling a second portion of the recesses with a semiconductor material 40A, 40B; wherein the stress imposing material is a material that introduces a compressive stress; wherein the stress imposing material is a material that introduces a tensile stress; wherein the stress imposing material is a material that introduces a stress that degrades electron or hole mobility in the semiconductor structure; wherein the stress imposing material is a material that introduces a stress that enhances electron or hole mobility in the semiconductor structure (col. 2, line 23-col. 4, line 44). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of forming recesses in a substrate, filling a first portion of recesses with a stress imposing material, and filling a second portion of the recesses with a semiconductor material, as taught by Murthy to incorporate into and modify the Gardner's method to include the Murthy's teachings to arrive the claimed limitations in order to provide a semiconductor transistor having a stressed channel.

Regarding Claim **5**, Gardner and Murthy disclose the claimed limitations except for the depth of the recess area is about 150 to 2000 angstroms. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the depth of the recess has a depth of about 500 to 2000 angstroms, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding Claim **9**, Gardner discloses in Fig. 9 the recesses/openings are substantially equidistant from the gate.

Regarding Claims **14-15, 36 and 37**, Murthy discloses the stress imposing material is made of silicon germanium col. 3, line 43), and the semiconductor material is made of epitaxially grown Si (col. 3, line 21). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the stress imposing material made of silicon germanium, and the semiconductor material made of epitaxially grown Si, as taught by Murthy in order to provide a semiconductor transistor having a stressed channel.

Regarding Claims **16, 17 and 25**, Murthy discloses the stress imposing material is a material that introduces a tensile stress or a compressive stress. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the stress imposing material/the stress-inducing layer is a material that introduces a tensile stress or a compressive stress since it was known in the art that the stress imposing material/the stress-inducing layer is a material that introduces a tensile stress in a direction parallel to a direction of current flow for the n-channel field effect transistor gate, and the stress imposing material is a material that introduces a compressive stress in a direction parallel to a direction of current flow for the p-channel field effect transistor gate.

Regarding Claim **18**, Murthy discloses a method further comprising a step of annealing after filling the first portion of the first recess and the first portion of the second recess with a stress imposing material (col. 3, lines 40-47). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to carry out a step of annealing after filling the first portion of the first recess and the first portion of the second recess with a stress imposing material to cause diffusion of the regions into the substrate.

Regarding Claims **24 and 31-35**, Gardner discloses in Figs. 7-11 and the corresponding texts as set forth in column 6, line 40-column 9, line 29, a method of forming a semiconductor structure comprises steps of:

forming a field effect transistor gate 44 on a substrate 30;

forming a first dummy spacer 52 and a second dummy spacer 52 on sides of the field effect transistor gate;

forming a mandrel/dielectric layer 34 with portions of the mandrel/dielectric layer abutting the first and second dummy spacers for the field effect transistor gate;

after masking the semiconductor structure, introducing stress to the field effect transistor gate; and

removing the mandrel/dielectric layer.

wherein the step of introducing stress material comprises:

removing the first and second dummy spacers from the field effect transistor gate to form first and second spacer voids 46 between the field effect transistor gate and the portions of the mandrel/dielectric layer;

creating a first recess 48 in the substrate below and in alignment with the first spacer void and a second recess 48 in the substrate below and in alignment with the second spacer void for the field effect transistor gate; and

unmasking the semiconductor structure.

Gardner fails to teach the step of introducing stress material comprises:

filling a first portion of the first recess and a first portion of the second recess with a stress imposing material configured to enhance performance of the field effect transistor gate; and

filling a second portion of the first recess and a second portion of the second recess for the field effect transistor gate with a semiconductor material.

Murthy teaches in Figs. 5-7 a method of forming a semiconductor transistor having a stressed channel comprising filling a first portion of recesses with a stress imposing material 22A, 22B; and filling a second portion of the recesses with a semiconductor material 40A, 40B; wherein the stress imposing material is a material that introduces a compressive stress; wherein the stress imposing material is a material that introduces a tensile stress; wherein the stress imposing material is a material that introduces a stress that degrades electron or hole mobility in the semiconductor structure; wherein the stress imposing material is a material that introduces a stress that enhances electron or hole mobility in the semiconductor structure (col. 2, line 23-col. 4, line 44). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of forming recesses in a substrate, filling a first portion of recesses with a stress imposing material, and filling a second portion of the recesses with a semiconductor material, as taught by Murthy to incorporate into and modify the Gardner's method to include the Murthy's teachings to arrive the claimed limitations in order to provide a semiconductor transistor having a stressed channel.

Claims **2 and 6-8** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gardner et al. (USP 6,111,292 hereinafter referred to as "Gardner") in view of Murthy et al. (US 6,621,131 hereinafter referred to as "Murthy"), and further in view of Yu (USP 6,297,117).

Regarding Claim **2**, Gardner and Murthy disclose all the claimed limitations except for a method further includes forming dummy spacers between the mandrel layer and the gate and forming a nitride interface as an etch stop in the recesses. Yu teaches in Fig. 5 that a method for forming a field effect transistor comprises forming dummy spacers 224, 226 between the mandrel/insulating layer 230 and the gate 208 and forming a nitride/liner oxide interface 228 (col. 5, lines 21-31). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form dummy spacers between the mandrel/insulating layer and the gate and forming a nitride/liner oxide interface, as taught by Yu in order to provide a smooth transition between the dummy spacers and the sidewalls of the gate structure (col. 5, lines 26-28).

Regarding Claims **6-8**, Gardner and Murthy disclose all the claimed limitations except for a method further comprises forming dummy spacers and removing the dummy spacers to form the spacer voids, wherein: a first dummy spacer has a first width; a second dummy spacer has a second width; a first recess of the recesses has a width substantially equal to the first width of the first dummy spacer; and a second recess of the recesses has a width substantially equal to the second width of the second dummy spacer, wherein the first width is substantially equal to the second width; and wherein the first width is about 100 to1000 Å. Yu teaches in Figs. 5-6 that a method for forming a field effect transistor further comprises forming dummy spacers 224, 226

and removing the dummy spacers to form the spacer voids/openings 232, 234, wherein a first dummy spacer 224 has a first width; a second dummy spacer 226 has a second width, and wherein the first width is substantially equal to the second width (col. 5, line 50-col. 6, line 4). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form dummy spacers and removing the dummy spacers to form the spacer voids/openings, wherein a first dummy spacer has a first width; a second dummy spacer has a second width and wherein the first width is substantially equal to the second width, as taught by Yu to incorporate into Gardner and Murthy's methods to further include forming dummy spacers and removing the dummy spacers to form the spacer voids, wherein: a first dummy spacer has a first width; a second dummy spacer has a second width; a first recess of the recesses has a width substantially equal to the first width of the first dummy spacer; and a second recess of the recesses has a width substantially equal to the second width of the second dummy spacer since it was known in the art that processes for forming such first and second dummy spacers are known to one of ordinary skill in the art of integrated circuit fabrication (col. 28-31). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the first width is about 100 to1000 Å, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Claims **19-22** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (USP 6,297,117) in view of Gardner et al. (USP 6,111,292 hereinafter referred to as "Gardner") further in view of Murthy et al. (US 6,621,131 hereinafter referred to as "Murthy").

Regarding Claims **19-20**, Yu discloses in Figs. 5-6 and the corresponding texts as set forth in column 5, line 50-column 6, line 4, a method of forming a semiconductor structure comprises steps of:

forming first dummy spacers 224, 226 on sides of a gate 208 formed on a substrate 204;

forming a mandrel/insulating layer 230 with portions of the mandrel/insulating layer abutting the dummy spacers; and

removing the dummy spacers to form spacer voids/openings 232, 234 between the gate and mandrel/insulating layer.

Yu fails to teach a method of forming a semiconductor structure comprises steps of creating recesses in the substrate below and in alignment with the spacer void; filling a first portion of the recesses with a stress imposing material; and filling a second portion of the recesses with a semiconductor material. Gardner discloses in Figs. 7-11 and the corresponding texts as set forth in column 6, line 40-column 9, line 29, a method of forming a semiconductor structure comprises steps of forming spacer voids/openings 46 between a gate 44 and a mandrel/dielectric layer 34; creating recesses/LDD areas 48 in a substrate 30 below and in alignment with the spacer voids/the openings, removing the mandrel/dielectric layer. Gardner fails to teach a method of forming a semiconductor structure comprises steps of filling a first portion of recesses with a stress imposing material; and filling a second portion of the recesses with a semiconductor material. Murthy teaches in Figs. 5-7 a method of forming a semiconductor transistor having a stressed channel, comprises the steps of forming recesses 36A, 36B in a substrate 10; filling a first portion of recesses with a stress imposing material 22A, 22B; and filling a second portion of the recesses with a semiconductor material 40A, 40B (col. 2, line

23-col. 4, line 44). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of forming recesses in a substrate, filling a first portion of recesses with a stress imposing material, and filling a second portion of the recesses with a semiconductor material, as taught by Murthy to incorporate into and modify the Yu and Gardner's method to include the Murthy's teachings to arrive the claimed limitations in order to provide a semiconductor transistor having a stressed channel.

Regarding Claim **21**, Murthy discloses the stress imposing material is made of silicon germanium col. 3, line 43). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the stress imposing material made of silicon germanium, as taught by Murthy in order to provide a semiconductor transistor having a stressed channel.

Regarding Claim **22**, Murthy discloses the stress imposing material/the stress-inducing layer is a material that introduces a tensile stress or a compressive stress. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to use the stress imposing material/the stress-inducing layer is a material that introduces a tensile stress or a compressive stress since it was known in the art that the stress imposing material/the stress-inducing layer is a material that introduces a tensile stress in a direction parallel to a direction of current flow for the n-channel field effect transistor gate, and the stress imposing material is a material that introduces a compressive stress in a direction parallel to a direction of current flow for the p-channel field effect transistor gate.

Claims **38-47** are rejected under 35 U.S.C. 103(a) as being unpatentable over Yu (USP 6,297,117) in view of Murthy et al. (US 6,621,131 hereinafter referred to as "Murthy").

Regarding Claims **38-40, 42, 45 and 46**, Yu discloses in Figs. 5-6 and the corresponding texts as set forth in column 5, line 50-column 6, line 4, a method of providing compressive or tensile imposing materials selectively beneath and in alignment with spacer areas of a semiconductor substrate and adjacent to channel areas to enhance electron and hole mobility in CMOS circuits, comprising:

forming disposable dummy spacers 224, 226 on the semiconductor substrate 204 and adjacent to the channel areas of a patterned gate 208;

forming a mandrel/an insulating layer 230 over active device regions of the patterned gate, abutting the disposable dummy spacers; and

after forming of the mandrel, removing the disposable dummy spacers to form spacer voids/openings 232, 234.

Yu fails to teach the method comprising etching recesses into the semiconductor substrate at a bottom of the spacer voids; introducing a compressive or tensile imposing material into a portion of the recesses; and filling a remainder of the recesses with material. Murthy teaches in Figs. 5-7 a method of forming a semiconductor transistor having a stressed channel, comprises the steps of forming recesses 36A, 36B in a substrate 10; filling a first portion of recesses with a stress imposing material 22A, 22B; and filling a second portion of the recesses with a semiconductor material 40A, 40B; wherein the stress imposing material is a material that introduces a compressive stress; wherein the stress imposing material is a material that introduces a tensile stress; wherein the stress imposing material is a material that introduces a stress that degrades electron or hole mobility in the semiconductor structure; wherein the stress imposing material is a material that introduces a stress that enhances electron or hole mobility in

the semiconductor structure (col. 2, line 23-col. 4, line 44). It would have been obvious to one of ordinary skill in the art at the time of the invention was made to utilize the teachings of forming recesses in a substrate, filling a first portion of recesses with a stress imposing material, and filling a second portion of the recesses with a semiconductor material, as taught by Murthy to incorporate into and modify the Yu's method to include the Murthy's teachings to arrive the claimed limitations in order to provide a semiconductor transistor having a stressed channel.

Regarding Claims **41 and 47**, Yu and Murthy disclose the claimed limitations except for the depth of the recess area is about 150 to 2000 angstroms; the tensile imposing material is annealed by rapid thermal annealing (RTA) between 950 to 1050°C. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to form the depth of the recess has a depth of about 500 to 2000 angstroms; and to anneal the tensile imposing material by rapid thermal annealing (RTA) between 950 to 1050°C, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

Regarding Claims **43-44**, Yu discloses the disposable dummy spacers are comprised of a nitride; the disposable dummy spacers are comprised of a SiO_2 liner and a polysilicon film (col. 5, lines 20-31).

Conclusion

A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to become abandoned (see M.P.E.P 710.02(b)).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Andy Huynh, (571) 272-1781. The examiner can normally be reached on Monday-Friday from 8:30 AM to 5:00 PM. The Fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the -status of this application or proceeding should be directed to the receptionist whose phone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Andy Huynh
Patent Examiner